Remarks

Claims 1-14 are currently pending in the subject application (claims 3 and 4 are withdrawn from consideration) and claims 1, 2 and 5-14 are presently under consideration. Claims 1, 2, 5, 6 and 13 have been amended herein. The specification has been amended at the second full paragraph at page 5, lines 18 to 24 of the specification. A clean version of the replaced paragraph and all pending claims is found at pages 2-4 of this Reply. Favorable reconsideration is requested in view of the comments and amendments made herein.

I. Informalities of Disclosure

The disclosure is objected to because of the following informalities: On page 5, line 21, "area between 8" before "the two polysilicon lines 4." should be replaced with --area 8 between --. On page 6, line 1, "forms the 12'" should be replaced with --forms spacer 12'--. Applicants have amended the paragraph at page 5, line 21 to read --area 8 between--.

Applicants have noted that some confusion may have arisen over the proper application of the previously filed preliminary amendment introducing corrections at page 6, line 1. The correction was to be applied to the second occurrence of "spacer" and not the first occurrence of spacer. Thus, page 6, line 1, after application of the preliminary amendment, should read "**forms the spacer 12'. Following the formation of spacer 12', a portion of the gate oxide may**". Applicants' representative respectfully request that the preliminary amendment be applied in such manner. This would directly address Examiner's concern regarding this line of the specification.

II. Rejection of Claims 1, 2, and 5-14 Under 35 U.S.C. §112

Claims 1, 2, and 5-14 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Independent claims 1, 5 and 13 have been amended herein pursuant to the Examiner's suggestions, and such amendments are believed to cure any indefiniteness with respect to the subject claims. Accordingly, withdrawal if this rejection is respectfully requested.

III. Rejection of Claims 1, 2, and 5-14 Under 35 U.S.C. 102(e)

Claims 1, 2, and 5-14 stand rejected under 35 U.S.C. 102 (e) as being anticipated by Nakajima, *et al.* (U.S. Patent 5,329,482). Applicants' representative respectfully traverses this rejection and submits that it should be withdrawn for at least the following reasons. Nakajima, *et al.* does not disclose each and every element recited in the respective claims.

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The claimed invention relates to a method of fabricating dual insulating spacers located adjacent to polysilicon lines in a nonvolatile memory cell and its peripheral circuitry. During spacer deposition for periphery devices, the space between adjacent polysilicon lines may be filled in the core region. This material undesirably prevents subsequent implants from occurring between the adjacent polysilicon lines in the core region. Thus, one instance of the present invention involves a process for forming dual spacers which allows an intermediate ion implant step between a first and second spacer formation step.

Contrary to the Examiner's assertion, Nakajima, *et al.* neither discloses nor suggests the subject invention and in particular the aforementioned claimed features. Nakajima, *et al.* relates to an invention having a polysilicon line in a core area and a polysilicon line in a periphery area. It provides a method to construct transistors in each of these areas by alternating resist patterns between the core and periphery areas. It does not disclose any means or process for providing doping ***between*** adjacent polysilicon lines ***in the same area***. Additionally, it does not even disclose adjacent polysilicon lines nor the space between adjacent polysilicon lines.

With respect to claims 1, 2 and 5-14, the Examiner references the Abstract section and Col. 5, lines 27-31 and 36-39 of Nakajima, *et al.* "Nakajima, *et al.* discloses depositing a first oxide layer 8 over at least two polysilicon lines 6 and 12 of each of a core and a periphery area, performing a first spacer etch in the core and periphery area, implanting an area 11 located between two polysilicon lines in the core area ...". Applicants submit that the polysilicon lines

referred to in Nakajima, *et al.* are directed to a single polysilicon line in the core area and a single polysilicon line in the periphery area. The core polysilicon line produces an offset transistor and the periphery polysilicon line produces a non-offset transistor. Applicants' representative can find no mention in the Examiner's cited parts of Nakajima, *et al.* nor in any other part that refers to implanting between two adjacent polysilicon lines in the core area. Likewise, no mention or suggestion is found in the reference of implantation between two adjacent polysilicon lines in the periphery area. Applicants' representative respectfully requests the Examiner to particularly point out where these features are disclosed in the reference. In the alternative, Applicants request that these rejections be withdrawn.

The Examiner also states, "Nakajima, *et al.* also teaches that the first oxide layer has a thickness of less than one-half the distance between a periphery of the adjacent polysilicon lines (Figure 5)." Applicants' claims have been amended to recite "distance between adjacent polysilicon lines". Nonetheless, Figure 5 of Nakajima, *et al.* in no way discloses any distances between adjacent polysilicon lines in the same area. Figure 5 is also not a scaled drawing and, therefore, no reasonable distances/measurements can be construed from this figure.

Although, Nakajima, *et al.* relates to a process for constructing MOS transistors for core and peripheral areas; it does not teach or suggest the above-noted features of the subject invention as recited in independent claims 1, 5, 12 and 13 (and claims 2, 6-11 and 14 which depend therefrom). This rejection should be withdrawn.

CONCLUSION

The present application is believed to be in condition for allowance in view of the amendments and comments herein. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

The Examiner is invited to contact Applicants' undersigned representative over the telephone to expedite favorable prosecution of the subject application.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Please amend the specification as follows:

Please replace the second full paragraph at page 5, lines 18 to 24 as follows:

In FIG. 1 shows a prior art non-volatile memory device 1 after polysilicon etching. Two polysilicon lines 4 are deposited on the substrate 3. FIG. 2 shows a prior art non-volatile memory device 1 after a first oxide layer 12 is deposited over and in the area 8 between [8] the two polysilicon lines 4. In FIG. 3, a prior art non-volatile memory device 1 is shown after performance of a first spacer etch showing the spacer 12' (where prime in the figures represents a spacer formed from the oxide layer deposition). Implantation occurs in implantation area 8'.

Page 5, line 21, please replace "area between 8" with --area 8 between--.

In the Claims:

Please amend claims 1, 2, 5, 6 and 13 as follows:

1. (Amended) A method for forming a spacer, comprising:

depositing a first oxide layer over at least two adjacent polysilicon lines in each of a core area and a periphery area;

performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two adjacent polysilicon lines in the core area;

applying a second oxide layer over the core area and the periphery area[s]; and

performing a second spacer etch over the periphery area[wherein a different appearance of the core and periphery areas is produced], the core area retaining an amount of the second oxide between the adjacent polysilicon lines while the periphery area is deplete of the second oxide between its adjacent polysilicon lines.

2. (Amended) The method of claim 1 wherein the first oxide layer has a thickness of less than one-half the distance between [a periphery of]adjacent polysilicon lines.

5. (Amended) A process for fabricating a non-volatile memory device comprising:

providing a substrate having a core area, a periphery area, and at least two adjacent polysilicon lines [overlying] in each of the core area and the periphery area;

depositing a first oxide layer over the adjacent polysilicon lines;

performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two adjacent polysilicon lines in the core area;

depositing a second oxide layer over the core area and the periphery area[s]; and

performing a second spacer etch over the periphery area.

6. (Amended) The process of claim 5, wherein the first oxide layer has a thickness of less than one-half the distance between[a periphery of] adjacent polysilicon lines.

13. (Amended) A process for fabricating a memory cell comprising the steps of:

providing a substrate having a core area, a periphery area, at least two adjacent polysilicon lines [overlying]in each of the core area and the periphery area, and first spacers adjacent [the]at least two adjacent polysilicon lines [overlying]in each of the core area and the periphery area; and

forming a second spacer adjacent at least one first spacer.